## REMARKS

Claims 11 to 20 are now pending in the present application. Applicants respectfully request reconsideration of the present application in view of the following remarks.

Applicants thank the Examiner for the indication that the objections to the specification, drawings, and claims, and the claim rejections under 35 U.S.C. §112, have been withdrawn.

Claims 11, 12, and 20 were rejected under 35 U.S.C. §102(b) as anticipated by U.S. Patent No. 6,199,184 (the "Sim" reference).

Claim 11 relates to a device for forming a signature. Claim 11, as presented, provides a shift register having a number of bit position memory devices to which input data to be tested is applied and a code generator which generates at least one additional bit position in at least one ***additional bit position memory device of the shift register*** from each applied data word in the signature.

The Office Action, at section three (3), cites the "Sim" reference at Figure 4, 42-2 as disclosure of the code generator as well as the "at least one additional shift register." As an initial matter, this assertion does not consider the amendments of Applicants' Response, filed on December 18, 2007. On page two (2) of that paper, Applicants' amended claim 11, in pertinent part, to recite "a code generator which generates at least one additional bit position in at least one additional bit position memory device of the shift register from each applied data word in the signature." Reconsideration of this rejection is respectfully requested, in light of Applicants' amendment of December 18, 2007.

The "Sim" reference does not disclose a code generator which generates at least one additional bit position in at least one additional bit position memory device of the shift register. In Figure 4 of the "Sim" reference, MISRs 42-1 and 42-2 are two distinct shift registers coupled in series. The "Sim" reference makes this clear, for example, at column 4, lines 63 to 64 ("[t]he compression circuit 40 includes first and second 6-bit MISRs 42-1 and 42-2 coupled in series.") and at column 5, lines 19 to 21 ("[a]n input of the XOR gate 47-i [of 42-2] is fed with a corresponding bit of the output [to which the Examiner apparently refers as disclosing a signature] from the first MISR 42-1."). In contrast, the present invention features a shift register and a "code generator which generates at least one additional bit position in at least one additional bit position memory device of the shift register." The present invention describes, for example, with respect to Figure 4, a code generator of i bits,

and additional bit position memory devices, or flip-flops, provided for each of the i bits or an additional bit position memory device for a formed parity bit. In the description of Figure 4 of the present invention, for example, at paragraphs [0014] and [0021], the MISR is extended by an i bit code generator 407 and at least one additional flip-flop. The code generator and shift register structure of the present invention is not the same as the dual MISR structure of the "Sim" reference. Therefore, the MISR 42-2 of the "Sim" reference does not identically disclose, or even suggest, a component which "generates at least one additional bit position in at least one additional bit position memory device of the shift register" as provided for in the context of claim 11.

For at least these reasons, the "Sim" reference does not identically disclose, or even suggest, each feature of claim 11, so that the "Sim" reference does not anticipate claim 11 or any of its dependent claims, e.g., claim 12.

Claim 20, as presented, includes subject matter analogous to that of claim 11, so that the "Sim" reference does not anticipate claim 20 for at least essentially the same reasons set forth above in support of the patentability of claim 11.

Withdrawal of this anticipation rejection is therefore respectfully requested.

Claim 13 was rejected under 35 U.S.C. §103(a) as obvious over the "Sim" reference.

Claim 13 depends from claim 11 and therefore includes all of the features of claim 11. As set forth in the patentability of claim 11, the "Sim" reference does not disclose or suggest the claim feature of a code generator which generates at least one additional bit position in at least one additional bit position memory device of the shift register from each applied data word in the signature, as provided for in the context of claim 11 from which claim 13 depends.

For at least these reasons, the "Sim" reference does not disclose or suggest each feature of claim 13, so that claim 13 is allowable.

Further, claim 13 is directed to a device according to claim 11, wherein the individual bit position memory devices are connected by equivalence points, and the individual bits of the data words, as well as the at least one additional bit position of the code generator, are inserted at the equivalence points to form the signature. The Office Action, at section four (4), asserts that "[t]he use of an inverted XOR position (equivalence point) has not been claimed by the applicant as having a patentable distinction or feature that would distinguish the device from other devices." As disclosed, for example, in paragraph [0021] of

the specification, use of an equivalence gate, instead of an antivalence gate, achieves a considerably lower error masking probability. This result shows the criticality of the claimed arrangement. Therefore, this is a significant feature and not merely a design choice.

Claims 14 to 19 were rejected under 35 U.S.C. §103(a) as obvious over the "Sim" reference in view of Biswas, "Design of UED-AUED Codes from Berger's AUED Code," IEEE VLSI Design, pages 364-369 (the "Biswas" reference).

Claims 14 to 19 ultimately depend from claim 11 and therefore include all of the features of claim 11. Accordingly, the combination of the "Sim" and "Biswas" references does not render unpatentable these dependent claims for at least the same reasons set forth above in support of the patentability of claim 11, since the secondary "Biswas" reference does not correct the critical deficiencies of the "Sim" reference noted above in support of the patentability of claim 11.

Withdrawal of this obviousness rejection is therefore respectfully requested.

## CONCLUSION

In view of the foregoing, it is respectfully submitted that all of claims 11 to 20 are allowable. It is therefore respectfully requested that the objections and rejections be withdrawn. Prompt reconsideration and allowance of the present application are therefore respectfully requested.

Respectfully submitted,

KENYON & KENYON LLP

Dated: April 28, 2008

By: /[signature]/ (Reg. No. 59,210) for:
Gerard A. Messina
(Reg. No. 35,952)

One Broadway
New York, NY 10004
(212) 425-7200
**CUSTOMER NO. 26646**